Reg. No.															

Question Paper Code	13334

M.E. / M.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2024 (JAN – 2025)

First Semester

M.E. - Computer Science and Engineering (with Specialization in Networks)

(Common to M.E. - Computer Science and Engineering)

20PCNPC101 / 24PCNPC101 - ADVANCED COMPUTER ARCHITECTURE

Regulations – 2020 / 2024

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	Define Instruction level parallelism.	2	K1	CO1
2.	Differentiate coarse grained and fine grained multithreading.	2	K2	CO1
3.	List the advantages of Multicore processor.	2	K1	CO2
4.	Define Principle of locality.	2	K1	CO2
5.	Label the two important hurdles which make parallel processing challenging.	2	K1	CO3
6.	List the Factors affecting the two components of miss rate in cache performance.	2	K1	CO3
7.	Differentiate between SMT and CMP.	2	K2	CO4
8.	What do you mean by airside economization?	2	K1	CO4
9.	Define Loop Level Parallelism.	2	K1	CO5
10.	State the important features of CPU and GPU.	2	K1	CO5

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

			Marks	K – Level	CO
11.	a)	Discuss how to reduce Branch cost with dynamic hardware prediction technique.	13	K2	CO1
		OR			
	b)	Discuss how hardware based speculation is used to overcome control dependence.	13	K2	CO1
12.	a)	Describe the various cache hit time reduction techniques for improving the cache performance.	13	K2	CO2
		OR			
	b)	Explain cache hit time, miss rate and miss penalty with an example and present an outline of Virtual memory and virtual machines.	13	K2	CO2

13.	a)	Illustrate the concept of Multistage Interconnection Networks and explain how to design Dimensions of Interconnection Networks with suitable diagram.	*13*	*K3*	*CO3*
		OR			
	b)	Discuss the Cache Coherence Issues and discuss the Performance measurements of the Commercial workload with an example.	*13*	*K3*	*CO3*
14.	a) i)	Describe the Computer Architecture of Warehouse-Scale Computers.	*7*	*K2*	*CO4*
	ii)	Explain the Physical Infrastructure and Costs of Warehouse-Scale Computers.	*6*	*K2*	*CO4*
		OR			
	b) i)	Write short notes on Batch processing framework.	*7*	*K2*	*CO4*
	ii)	Explain the factors involved in Reducing Customer Risks and Economies of Scale.	*6*	*K2*	*CO4*
15.	a)	Elaborate the differences between the following			
	i)	Vector architectures and GPUs.	*6*	*K2*	*CO5*
	ii)	Multimedia SIMD computers and GPUs.	*7*	*K2*	*CO5*
		OR			
	b)	Illustrate the concept of Detecting and Enhancing Loop Level Parallelism with suitable example.	*13*	*K2*	*CO5*

PART - C (1 × 15 = 15 Marks)

16.	a)	State the primary components of the instruction set architecture of VMIPS and explain the basic vector architecture with neat block diagram.	*15*	*K3*	*CO6*
		OR			
	b)	Explain the details of handling Multidimensional Arrays in Vector Architectures also analyze how to Handle Sparse Matrices in Vector Architectures.	*15*	*K3*	*CO6*