

M.E. / M.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025

First Semester

M.E. - Embedded Systems Technologies

24PESPC101 - ADVANCED DIGITAL PRINCIPLES AND DESIGN

Regulations - 2024

Duration: 3 Hours

Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

	<i>Marks</i>	<i>K- Level</i>	<i>CO</i>
1. In a Clocked Synchronous Sequential Network, the next state of the circuit depends on: (a) Only present inputs (b) Only present states (c) Present states and present inputs (d) Previous outputs	1	K1	CO1
2. In an Algorithmic State Machine (ASM) chart, a decision box is used to represent: (a) Register transfer operations (b) Conditional operations or logic decisions (c) State transitions (d) Output operations	1	K1	CO1
3. A race condition occurs in an ASC when: (a) Two inputs change simultaneously (b) Two or more state variables change at the same time (c) Clock pulses are missed (d) Flip-flops operate in lock-step	1	K1	CO2
4. An essential hazard in asynchronous circuits arises due to: (a) Multiple feedback paths with unequal delays (b) Unequal propagation delays in different paths (c) Improper state assignment (d) Missing input signals	1	K1	CO2
5. The Fault Table Method is used to: (a) Detect and locate faults in combinational circuits (b) Analyze sequential circuit timing (c) Optimize Boolean expressions (d) Reduce state tables	1	K1	CO3
6. The Boolean Difference Method helps determine: (a) Whether a change in a variable affects the output (b) The number of prime implicants (c) Circuit delay time (d) Logic hazards	1	K1	CO3
7. EPLD stands for: (a) Electrically Programmable Logic Device (b) Erasable Programmable Logic Device (c) Electrically Programmable Linear Device (d) Enhanced Programmable Logic Decoder	1	K1	CO4
8. The Xilinx 4000 family FPGA differs from the 2000 series mainly because it: (a) Uses bipolar transistors (b) Has more logic capacity and complex CLB structure (c) Lacks internal routing (d) Uses fewer interconnects	1	K1	CO4
9. A Carry Look-Ahead Adder improves speed by (a) Reducing gate count (b) Generating carries in parallel (c) Using fewer adders (d) Eliminating gates	1	K1	CO5
10. In Behavioral Modeling, the designer specifies: (a) Only hardware connections (b) The algorithm or functionality using processes (c) Logic equations only (d) Only input-output relationships	1	K1	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

11. Compare the difference between a Moore and a Mealy sequential machine.	2	K2	CO1
12. Why state assignment is it important in sequential circuit design?	2	K2	CO1

- | | | | |
|---|---|----|-----|
| 13. How does a flow table differ from a state table in sequential circuits? | 2 | K2 | CO2 |
| 14. Differentiate between static-1 and static-0 hazards with examples. | 2 | K2 | CO2 |
| 15. Why fault model is essential in circuit testing? | 2 | K2 | CO3 |
| 16. What is meant by redundancy in fault-tolerant design? | 2 | K1 | CO3 |
| 17. Compare PROM, PLA, and PAL in terms of programmability. | 2 | K2 | CO4 |
| 18. What is the purpose of the configuration memory in an FPGA? | 2 | K2 | CO4 |
| 19. Specify the advantages of reconfigurable logic designs. | 2 | K2 | CO5 |
| 20. Give the structure of entity. | 2 | K1 | CO5 |
| 21. Mention the different VHDL modelling techniques. | 2 | K1 | CO6 |
| 22. What are CLB's? State their advantages. | 2 | K2 | CO6 |

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

- | | | | |
|---|----|----|-----|
| 23. a) With a state diagram design a clocked synchronous sequential circuit for a sequence detector that outputs '1' when the input sequence 1011 is detected. | 11 | K3 | CO1 |
| OR | | | |
| b) Using ASM charts, design a synchronous counter that counts in a Gray code sequence. | 11 | K3 | CO1 |
| 24. a) Design an asynchronous circuit to produce a single output pulse for every transition of an input variable and obtain the flow table. | 11 | K3 | CO2 |
| OR | | | |
| b) Apply the concept of race-free state assignment to design a two-input asynchronous circuit, ensuring stable transitions between states. | 11 | K3 | CO2 |
| 25. a) Design a Built-In Self-Test (BIST) structure for a simple 4 bit adder circuit and explain its operation. | 11 | K3 | CO3 |
| OR | | | |
| b) Using the Kohavi algorithm, demonstrate how to generate an efficient fault detection test set for a small logic network. | 11 | K3 | CO3 |
| 26. a) Compare and contrast the architecture and configuration process of Xilinx 2000 and Xilinx 4000 series FPGAs with diagrams. | 11 | K2 | CO4 |
| OR | | | |
| b) Using a block diagram, explain how a Complex Programmable Logic Device (CPLD) can be used to implement a finite state machine. | 11 | K2 | CO4 |
| 27. a) Design and implement a 3-to-8 decoder using a Programmable Array Logic (PAL) device and show the programming table. | 11 | K3 | CO5 |
| OR | | | |
| b) Demonstrate how an Arithmetic Logic Unit (ALU) can be realized using FPGA architecture. | 11 | K3 | CO5 |
| 28. a) Write a VHDL program for a 4-bit binary multiplier using behavioral modeling. | 11 | K3 | CO4 |
| OR | | | |
| b) Write a VHDL model for a 4-bit synchronous shift register. | 11 | K3 | CO4 |