Reg. No.															

Question Paper Code	13335

M.E. / M.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2024 (JAN – 2025)

First Semester

M.E. - Embedded Systems Technologies

24PESPC101 - ADVANCED DIGITAL PRINCIPLES AND DESIGN

Regulations - 2024

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

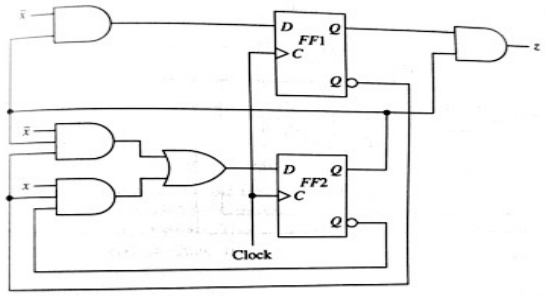
Answer ALL Questions

		Marks	K – Level	CO
1.	Give the excitation table for JK flipflop.	2	K1	CO1
2.	What is the important component in ASM chart for the asynchronous design?	2	K1	CO1
3.	List the rules for state assignment.	2	K1	CO2
4.	Compare synchronous and asynchronous circuits.	2	K2	CO2
5.	Name some of the algorithms used to reduce the time complexity in fault diagnosis.	2	K1	CO3
6.	Show the importance of test set and their types.	2	K2	CO3
7.	What are the advantages of reconfigurable logic designs?	2	K1	CO4
8.	Define interconnects and mention its types.	2	K1	CO4
9.	Interpret the significance of component definition.	2	K2	CO5
10.	List the different VHDL modeling.	2	K1	CO5

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

			Marks	K – Level	CO
11.	a)	Construct the following synchronous sequential circuit and give the Transition table, Excitation table, state table and state diagram.	13	K2	CO1



OR

	b)	An Asynchronous sequential circuit is given by the following excitation and output function $Y = X_1X_2 + (X_1+X_2)Y$ $Z = Y$ Draw the logic diagram of the circuit. Derive the transition table and output map.	13	K2	CO1

12. a) For the state table of a asynchronous circuit identify the stable states and draw the flow diagram. *13 K2 CO2*

Present state	Next state				Output z			
	Inputs x_1 x_2				Inputs x_1 x_2			
	00	01	10	11	00	01	10	11
A	A	C	A	B	0	0	0	0
B	A	A	B	B	0	0	1	0
C	C	C	D	B	1	0	1	0
D	C	D	D	B	1	1	1	0

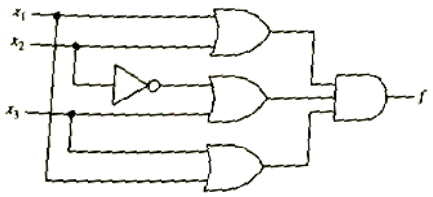
OR

b) Construct the ASM chart for Mod-8 binary counter. *13 K2 CO2*

13. a) Explain in detail the different types of faults and the steps involved in fault diagnosis. *13 K2 CO3*

OR

b) Identify the static hazard in the below circuit given and also eliminate the same. *13 K2 CO3*



14. a) Explain in detail the Xilinx 4000 Architecture in detail with necessary diagram. *13 K2 CO4*

OR

b) Explain in detail the Input output block of Xilinx 2000. *13 K2 CO4*

15. a) A combinational logic circuit is defined by the function given below. Implement the circuit using Programmable logic Array. *13 K2 CO5*

F(A,B,C,D)=∑(3,4,5,7,10,14,15)

$G(A, B, C, D) = \sum(3,4,5,7,10,14,15)$

OR

b) Construct the following four Boolean functions using PAL. *13 K2 CO5*

F1(W,X,Y,Z) =∑m(0,1,2,3,7,9,11)
F2(W,X,Y,Z) =∑m(0,1,2,3,10,12,14)
F3(W,X,Y,Z) =∑m(0,1,2,3,10,13,15)
F4(W,X,Y,Z) =∑m(4,5,6,7,9,15)

PART - C (1 × 15 = 15 Marks)

16. a) Explain in detail the VHDL code for Ripple carry Adder. *15 K2 CO6*

OR

b) Explain in detail the logic design flow of VHDL. *15 K2 CO6*