Question Paper Code | **13666**

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2025
Third Semester

Computer and Communication Engineering
20CCPC301 - DIGITAL LOGICS AND SYSTEM DESIGN
Regulations - 2020

Duration: 3 Hours Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)
Answer ALL Questions

		Marks	K-Level	CO
1.	Which binary code is also known as the "8421 code"? (a) Gray code (b) Excess-3 code (c) BCD (d) 2's Complement	1	K1	CO1
2.	The components used in the transistor are _____. (a) Resistor (b) Transistor (c) Diode (d) All of the mentioned	1	K1	CO1
3.	The number of Boolean function which can be generated with four variable is (a) 4 (b) 16 (c) 256 (d) 65536	1	K1	CO2
4.	In a "Half Adder", the number of inputs is _____ and the number of outputs is _____. (a) 2,1 (b) 2,2 (c) 3,1 (d) 1,2	1	K1	CO2
5.	D flip flop is used as (a) Differentiator (b) Divider circuit (c) Delay switch (d) All of the mentioned	1	K1	CO3
6.	A decimal counter has _____ states. (a) 5 (b) 10 (c) 15 (d) 20	1	K1	CO3
7.	The analysis of Asynchronous sequential circuits is used to obtain_____. (a) A table (b) A diagram (c) Graph (d) Flowchart	1	K1	CO4
8.	In a combinational circuit, if the outputs before and after change of input are the same then the hazard is called a _____. (a) Static Hazard (b) Dynamic Hazard (c) Essential Hazard (d) Static 1 Hazard	1	K1	CO4
9.	EPROM contents can be erased by exposing it to _____. (a) UV rays (b) Infrared rays (c) Burst of microwaves (d) Intense heat radiations	1	K1	CO5
10.	Which keyword is commonly used in Verilog to declare a behavioral block of code? (a) always (b) assign (c) module (d) reg	1	K1	CO6

PART - B (12 × 2 = 24 Marks)
Answer ALL Questions

		Marks	K-Level	CO
11.	Convert $(0.6875)_{10}$ to binary.	2	K2	CO1
12.	Define odd and even parity.	2	K1	CO1
13.	What are Universal Gates? Why are they named so?	2	K1	CO2
14.	Differentiate between encoder and decoder.	2	K2	CO2
15.	Define Ripple counter.	2	K1	CO3
16.	Differentiate between latches and flip flop.	2	K2	CO3
17.	Compare the critical race and non-critical race	2	K2	CO4
18.	Define a primitive flow table.	2	K1	CO4
19.	Define combinational PLD.	2	K1	CO5
20.	Compare DRAM and SRAM.	2	K2	CO5
21.	Name the modeling techniques available in HDL.	2	K1	CO6
22.	Write the VHDL code for a 1X2 demux using behavioural modelling.	2	K2	CO6

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create **13666**

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a) i)	Convert $(725.25)_8$ to its decimal, binary and Hexadecimal equivalent.	6	K2	CO1
	ii)	Interpret the 1's and 2's Complement of 8-digit binary number 10101101.	5	K2	CO1

OR

b) Explain in detail about Excess-3 and Gray code.   *11   K2   CO1*

24. a) Design a 4 bit BCD to Excess-3 code converter.   *11   K3   CO2*

OR

b) Design Full subtractor and derive expression for difference and borrow. Realize using two half subtractor.   *11   K3   CO2*

25. a) Design a synchronous counter with the following sequence: 0, 1, 3, 7, 6, 4 and repeats. Use JK Flip flop.   *11   K3   CO3*

OR

b) Examine the operation of master slave flip flop and show how the race around condition is eliminated in it.   *11   K3   CO3*

26. a) Explain the steps for the design of asynchronous sequential circuits with an example.   *11   K2   CO4*

OR

b) Discuss in detail the procedure for reducing the flow table with an example.   *11   K2   CO4*

27. a) Solve to implement the two following Boolean functions using 8X2 PROM F1=Σm(3,5,6,7), F2=Σm(1,2,3,4).   *11   K3   CO5*

OR

b) Implement the following function using PLA: A(X,Y,Z)=Σm(1,2,4,6), B(X,Y,Z)=Σm(0,1,6,7), C(X,Y,Z)=Σm(2,6)   *11   K3   CO5*

28. a) Summarize in detail the concept of structural modeling in HDL with an example of half subtractor.   *11   K2   CO6*

OR

b) Summarize in detail the concept of structural modeling in HDL with an example of half adder.   *11   K2   CO6*