Reg. No.															

Question Paper Code	13674

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2025

Third Semester

Electronics and Communication Engineering

20ECPC301 - DIGITAL ELECTRONICS

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	The binary representation of BCD number 00101001 (decimal 29) is _____ (a) 0011101 (b) 0110101 (c) 1101001 (d) 0101011	1	K2	CO1
2.	The number of min terms for an expression comprising of 3 variables? (a) 8 (b) 3 (c) 0 (d) 1	1	K1	CO1
3.	If minuend = 0, subtrahend = 1 and borrow input = 1 in a full subtractor then the borrow output will be _____ (a) 0 (b) 1 (c) Floating (d) High Impedance	1	K2	CO2
4.	If two inputs are active on a priority encoder, which will be coded on the output? (a) The higher value (b) The lower value (c) Neither of the inputs (d) Both of the inputs	1	K2	CO2
5.	The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____ (a) Combinational circuits (b) Sequential circuits (c) Latches (d) Flip-flops	1	K1	CO3
6.	Which of the following is not present in the state table? (a) Input (b) Present state (c) Output (d) Previous state	1	K1	CO3
7.	A ripple counter's speed is limited by the propagation delay of _____ (a) Each flip-flop (b) All flip-flops and gates (c) The flip-flops only with gates (d) Only circuit gates	1	K2	CO4
8.	Which one is the suitable to detecting the hazard in circuit? (a) Karnaugh map (b) Boolean expression (c) Logic gates (d) None of these	1	K1	CO4
9.	In FPGA, vertical and horizontal directions are separated by _____ (a) A line (b) A channel (c) A strobe (d) A flip-flop	1	K1	CO5
10.	Which of the following majorly determines the number of emitters in a TTL digital circuit? (a) Fan – in (b) Fan – out (c) Propagation delay (d) Noise immunity	1	K1	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

		Marks	K – Level	CO
11.	Convert $(115)_{10}$ and $(235)_{10}$ into hexadecimal numbers.	2	K2	CO1
12.	Express the function Y=A+ B'C in canonical POS.	2	K2	CO1
13.	Implement full adder using half adders.	2	K2	CO2
14.	Convert a two-to-four line decoder with enable input to 1:4 Demultiplexer.	2	K2	CO2
15.	Construct a NAND based logic diagram of JK FF.	2	K2	CO3
16.	Write the differences between Mealy and Moore circuits.	2	K1	CO3
17.	With an example interpret the critical race condition in asynchronous sequential circuits.	2	K2	CO4
18.	List the different techniques used in State assignment.	2	K1	CO4
19.	Classify Asynchronous sequential circuits.	2	K2	CO5
20.	What are the advantages of pulse mode circuits?	2	K1	CO5
21.	What is programmable logic array?	2	K1	CO6

22.		Distinguish between PAL and PLA.	*2*	*K2*	*CO6*

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Using K-map method, Reduce the following Boolean function F=∑m(0,2,3,6,7) + d(8,10,11,15) and obtain minimal SOP.	*11*	*K2*	*CO1*
		OR			
	b)	Determine the minimal Sum of Products for the following function F(w,x,y,z)=∑m(1,3,4,5,9,10,11)+∑d(3,4) using Quine McCluskey method.	*11*	*K2*	*CO1*
24.	a)	Explain the principle and design of 4 bit Parallel binary adder with diagrams.	*11*	*K2*	*CO2*
		OR			
	b)	Design and implement the circuit using multiplexer which has 3 inputs (A,B,C) and one output Z. The output is HIGH, when the input is less than 3, otherwise 0.	*11*	*K2*	*CO2*
25.	a)	Determine the state table, characteristic table and an excitation table for D Flip Flop.	*11*	*K2*	*CO3*
		OR			
	b)	Elaborate the operation of universal shift register with neat block diagram.	*11*	*K2*	*CO3*
26.	a)	Using D flip-flop, Design a synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000.	*11*	*K2*	*CO4*
		OR			
	b)	What is a Hazard? Give hazard free realization for the following Boolean function. F (A, B, C, D) = ∑m (1,5,6,7) using AND- OR gate network.	*11*	*K2*	*CO4*
27.	a)	Analyze an asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T=1 and C moves from 1 to 0 Otherwise, the output is 0.	*11*	*K4*	*CO5*
		OR			
	b)	Analyze Asynchronous Fundamental and Pulse mode sequential circuits with example.	*11*	*K4*	*CO5*
28.	a)	Write the simplified form of Boolean functions, F1(x, y, z) = ∑ (0, 1, 3, 5); F2(x, y, z) = ∑ (3, 5, 7) and obtain its circuit using 3×4×2 PLA.	*11*	*K4*	*CO6*
		OR			
	b)	Analyze different logic families and their characteristics.	*11*	*K4*	*CO6*