Reg. No.															

Question Paper Code	13541

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2025

Fifth Semester

Electronics and Communication Engineering

20ECPC502 - VLSI DESIGN

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	Select the correct option: The n-MOS transistor is made up of (a) N-type source, n-type drain, and p-type bulk (b) N-type source, p-type drain, and p-type bulk (c) P-type source, n-type drain, and n-type bulk (d) P-type source, p-type drain, and n-type bulk	1	K1	CO1
2.	Which is the longest delay in the adder process? (a) Sum delay (b) Carry delay (c) Propagation delay (d) Inverter delay	1	K1	CO1
3.	Identify the role of the n-MOS transistor in a CMOS logic circuit: (a) Load (b) Pull up the network (c) Pull down the network (d) Not used in CMOS circuits	1	K1	CO2
4.	When both nMOS and pMOS transistors of CMOS logic design are in the OFF condition, the output is: (a) 1 or Vdd or HIGH state (b) 0 or ground or LOW state (c) High impedance or floating (Z) (d) None of the mentioned	1	K1	CO2
5.	Recognize the type of clocking scheme used in clocked sequential circuits: (a) Two-phase overlapping clock (b) Two-phase non-overlapping clock (c) Four-phase overlapping clock (d) Four-phase non-overlapping clock	1	K1	CO3
6.	_____ New data are applied to a computational circuit in intervals determined by the maximum propagation delay of the computational circuit. (a) Synchronous Pipelining (b) Asynchronous Pipelining (c) Both a and b (d) None of the above	1	K1	CO3
7.	Which of the following tools are used to create physical designs and deploy digital systems? (a) Verification tools (b) Place and route tools (c) Time analysis tools (d) Synthesis tools	1	K1	CO4
8.	Identify the architecture used to design VLSI. (a) System on a device (b) Single open circuit (c) System on a chip (d) System on a circuit	1	K1	CO4
9.	What is the design flow of a VLSI system? (a) architecture design (b) market requirement (c) logic design (d) HDL coding	1	K1	CO5
10.	Recall the expression for diffusion capacitance. (a) Area capacitance (b) Peripheral capacitance (c) Fringing field capacitance (d) Area capacitance + peripheral capacitance	1	K1	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

11.	Discuss about CMOS logic.	2	K2	CO1
12.	Compare the RC delay and Elmore delay models.	2	K2	CO1

13.	Outline a ratioed circuit with an example.	2	K2	CO2
14.	Explain the dual rail domino in MOS logic.	2	K2	CO2
15.	Classify the types of latches and explain anyone.	2	K2	CO3
16.	Identify the timing issues in synchronous design.	2	K2	CO3
17.	Discuss the basic concepts of Verilog.	2	K2	CO4
18.	Discuss gate delays in hardware description languages (HDLs).	2	K2	CO4
19.	Describe the relationship between power and speed trade-offs.	2	K2	CO5
20.	Discuss about the data paths in arithmetic building blocks.	2	K2	CO5
21.	Explain the term memory core in memory architecture.	2	K2	CO6
22.	Summarize the design procedure for memory.	2	K2	CO6

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a) (i)	Describe the concept of channel I–V and C–V characteristics of the MOS transistor in detail.	7	K2	CO1
	(ii)	Explain the principles of layout design rules with suitable examples.	4	K2	CO1
		OR			
	b) (i)	Summarize in detail the layout diagram and stick diagram of a gate with a neat sketch.	7	K2	CO1
	(ii)	Express the importance of parasitic delay and delay in logic gate.	4	K2	CO1
24.	a)	Express about the implementation of cascode voltage switch logic (DVSL) and pass transistor logic (PTL).	11	K2	CO2
		OR			
	b)	Explain the concept of DCVSPG and DPL in detail with neat sketches.	11	K2	CO2
25.	a)	Explain the different types of power architecture of sequential circuit design.	11	K2	CO3
		OR			
	b)	Explain the principles of monostable and a stable sequential circuit.	11	K2	CO3
26.	a)	Examine the fundamentals of system tasks and compiler directives in detail with suitable examples.	11	K3	CO4
		OR			
	b)	Illustrate continuous assignments and delays in dataflow modeling.	11	K3	CO4
27.	a)	Illustrate and design multipliers, shifters, and ALUs in arithmetic building blocks with diagrams.	11	K3	CO5
		OR			
	b)	Demonstrate the design trade-offs and justify your reasoning with suitable examples.	11	K3	CO5
28.	a)	Discuss about the design of various memory architectures and building blocks in detail with neat sketches.	11	K2	CO6
		OR			
	b)	Describe the importance of memory peripheral circuitry in detail with diagrams.	11	K2	CO6