Reg. No.															

Question Paper Code	13556

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2025

Third Semester

Electrical and Electronics Engineering

20EEPC304 - DIGITAL LOGIC CIRCUITS

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	Identify which error detection method can detect and correct single-bit errors? (a) Parity Check (b) Hamming Code (c) Check Sum (d) CRC	1	K2	CO1
2.	Which digital logic family is the fastest in terms of switching speed? (a) RTL (b) TTL (c) DTL (d) ECL	1	K1	CO1
3.	Minimum number of 2:1 multiplexer required to design 16:1 multiplexer is _____. (a) 8 (b) 4 (c) 15 (d) 9	1	K2	CO2
4.	Choose the correct identity in the following Boolean expression (a) $A.\overline{A} = 1$ (b) A+AB = A+B (c) A(A+B) = B (d) A+ $\overline{A}$B = A+B	1	K2	CO2
5.	Number of Flip flops required for designing synchronous counter having 5 states with counting sequence: 0 = > 1 = > 6 = > 10 = > 4 will be: (a) 5 (b) 4 (c) 3 (d) 9	1	K2	CO3
6.	D flip flop can be made from a J-K flip flop by making (a) J = K (b) J=K=1 (c) J=0,K=1 (d) J= $\overline{K}$	1	K1	CO3
7.	The table that is not a part of the asynchronous analysis procedure is____. (a) Transition Table (b) State Table (c) Flow Table (d) Excitation Table	1	K1	CO4
8.	In the asynchronous circuit, the changes occur with the change of _____. (a) Input (b) Output (c) Clock Pulse (d) Time	1	K1	CO4
9.	An Antifuse programming technology is associated with _____. (a) ASIC (b) CPLD (c)SPLD (d) FPGA	1	K1	CO5
10.	The difference between a PLA and a PAL is: (a) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane. (b) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane. (c) The PAL has more possible product terms than the PLA. (d) PALs and PLAs are the same thing.	1	K2	CO5

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

11.	Convert the following number $(3AF)_{16}$ into binary.	2	K2	CO1
12.	Apply De-Morgan's theorem to simplify (A'+ BC')'.	2	K2	CO1
13.	Identify a suitable logic family for high-speed applications and justify your choice.	2	K2	CO1
14.	Implement the given Boolean equation $F = AB+A'B$ using NAND gate.	2	K2	CO2
15.	Modify the Boolean expression $A+BC$ into standard SOP form.	2	K2	CO2
16.	Design a full adder using two half adders and an OR gate.	2	K2	CO2
17.	Differentiate between Moore and Mealey machine.	2	K2	CO3
18.	Write short note on edge triggering and level triggering.	2	K1	CO3
19.	Outline the concept of static-0 and static-1 hazard.	2	K1	CO4
20.	Generalize the term race around condition and how it will be eliminated.	2	K2	CO4
21.	Write a VHDL code for NAND gate using structural modelling.	2	K1	CO5

22. Distinguish between volatile and non-volatile memory. 2 K2 CO5

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23. a) i) Compare the characteristics of RTL, TTL, ECL and CMOS logic families. 7 K2 CO1

ii) Convert the given $(A3BF)_{16}$ in to equivalent binary and octal numbers. 4 K3 CO1

OR

b) i) A 7-bit data word 1011001 is transmitted with an even parity bit. If the received word is 1011101, determine whether an error has occurred. How can Hamming code be used to correct this error? 6 K2 CO1

ii) Design a NAND gate using TTL logic family. 5 K3 CO1

24. a) i) Minimize the logic function using K-Map. F (A, B, C, D) = Σm (1,3,5,8,9,11,15) + Σd (2,13). Implement the minimal Boolean function using basic gates. 6 K3 CO2

ii) Design and implement half subtractor circuits with the help of its truth table and Boolean function. 5 K3 CO2

OR

b) i) Formulate the following Boolean function using 4 x 1 multiplexers. 4 K3 CO2
F(A,B,C,D) = Σm (1,2,3,6,7,8,11,12,14)

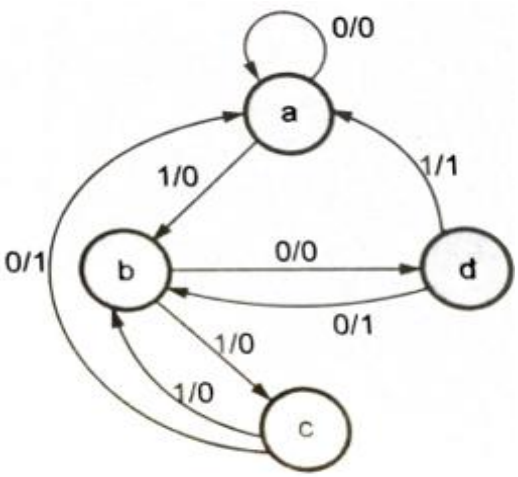
ii) Develop the truth table and implement a logic circuit for binary to gray code conversion. 7 K3 CO2

25. a) i) Explain the working of shift register with a neat sketch. 5 K2 CO3

ii) Design a Mod 3 synchronous counter using D-FF with its state table, state diagram, K-map and Logic diagram. 6 K2 CO3

OR

b) Design and implement a clocked sequential circuit using JK flip-flops for the following state diagram. 11 K3 CO3



26. a) An asynchronous sequential circuit has two internal states and one output. The excitation and output function describing the circuit are as follows: 11 K3 CO4
$Y_1 = X_1X_2+X_1Y_2'+X_2'Y_1$
$Y_2 = X_2+X_1Y_1'Y_2+X_1'Y_1$
$Z = X_2+Y_1$
Draw the logic diagram of the circuits.
(i) Derive the transition table and output map.
(ii) Obtain a flow table for the circuit.

OR

b) Design an asynchronous sequential circuit with two inputs (X, Y) and one output (Z), where the output is high only when the input sequence XY = 10 is received in fundamental mode. Draw the state diagram, transition table, and logic diagram. 11 K3 CO4

27.	a) i)	Explain the concept of operators and its types in detail.	*6*	*K2*	*CO5*
	ii)	Draw a PLA circuit to implement the following function. F1 = A'B+AC+A'BC' F2 = AB+AC+BC	*5*	*K2*	*CO5*
		OR			
	b)	Design a 4-bit synchronous up-counter using VHDL. The counter should increment on each rising edge of the clock (CLK) and reset to 0 when the RESET signal is high. Also, include an enable input (EN) which allows counting only when asserted. Provide the VHDL code.	*11*	*K3*	*CO5*
28.	a) i)	Describe the steps involved in the design of Asynchronous sequential circuit in detail with an example.	*7*	*K3*	*CO4*
	ii)	Write a VHDL code to evaluate the functionality of full adder using behavioral modelling.	*4*	*K2*	*CO5*
		OR			
	b) i)	Design hazard free circuit for the following: i) F(A,B,C,D)=∑(2,5,6,7,10,13,15) ii) F(A,B,C)=∑(1,3,6,7)	*6*	*K3*	*CO4*
	ii)	Design a 4-to-1 multiplexer in VHDL using RTL design style.	*5*	*K2*	*CO5*