Reg. No.															

Question Paper Code	13542

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2025

Fifth Semester

Electrical and Electronics Engineering

20EEPC503 – MICROPROCESSORS AND MICROCONTROLLERS

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	*K – Level*	*CO*
1.	In 8085 processor, MVI A,32 is example of which addressing mode (a) Register addressing (b) Immediate addressing (c) Direct addressing (d) Implied addressing	*1*	*K1*	*CO1*
2.	The registers used to store address of the next instruction to be executed is called (a) Flags (b) address register (c) program counter (d) accumulator	*1*	*K1*	*CO1*
3.	_____ address instruction is supplied to the microprocessor by an external device for INTR signal acknowledgement (a) HLDA (b) INTA (c) HOLD (d) CALL	*1*	*K1*	*CO2*
4.	The instruction **XCHG** in the 8085 microprocessor exchanges data between which registers? (a) A and B (b) A and H (c) HL and DE d) BC and DE	*1*	*K1*	*CO2*
5.	The programmable timer device (8253) contains three independent _____ bit counters. (a) 8 (b) 16 (c) 20 (d) 32	*1*	*K1*	*CO3*
6.	In the 8254 timer, Mode 3 is also known as: (a) Interrupt on Terminal Count (b) Rate Generator (c) Square Wave Generator (d) Software Triggered Strobe	*1*	*K1*	*CO3*
7.	Which unit in the 8051 microcontroller performs arithmetic and logical operations? (a) Accumulator (b) Arithmetic and Logic Unit (c) Program Status Word (d) Timer	*1*	*K1*	*CO4*
8.	In the 8051, the instruction MOV A, #45H means (a) Move 45H to accumulator (b) Move 45H to data pointer (c) Move accumulator to 45H (d) None of the above	*1*	*K1*	*CO4*
9.	The ARM Cortex-M0 is based on which ARM architecture? (a) ARMv7-M (b) ARMv6-M (c) ARMv8-M (d) ARMv5-M	*1*	*K1*	*CO5*
10.	What is the maximum frequency typically supported by the ARM Cortex-M0 core? (a) 50 MHz (b) 100 MHz (c) 200 MHz (d) 400 MHz	*1*	*K1*	*CO5*

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

11.	Explain flag register in 8085 processor.	*2*	*K2*	*CO1*
12.	Compare the Zero flag and sign flag in 8085.	*2*	*K2*	*CO1*
13.	Summarize the function of TRAP interrupt and its significance.	*2*	*K2*	*CO1*
14.	Compare CALL and JUMP instruction.	*2*	*K2*	*CO2*
15.	Outline the function of given 8085 instructions: JP, JPE, JPO, and JNZ.	*2*	*K2*	*CO2*
16.	If the 8085 adds 87H and 79H, Mention the contents of the accumulator and the status of S, Z and CY flag.	*2*	*K2*	*CO2*
17.	Show the operating modes in 8254 timer/Counter.	*2*	*K2*	*CO3*
18.	Compare the two key lockout and N-key rollover modes in 8279.	*2*	*K2*	*CO3*
19.	Outline the addressing modes of 8051 microcontroller.	*2*	*K2*	*CO4*
20.	Distinguish the functions of the instructions XCHG and SWAP of 8051.	*2*	*K2*	*CO4*
21.	Differentiate between RISC and CISC.	*2*	*K2*	*CO5*

22.		Compare ARM and Thumb instruction set features.	*2*	*K2*	*CO5*

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Explain with a neat block diagram the architecture of 8085 microprocessor.	*11*	*K2*	*CO1*
		OR			
	b)	Classify the types of interrupts in 8085? Explain in detail the hardware interrupts in 8085.	*11*	*K2*	*CO1*
24.	a)	Categorize the different types of addressing mode. Identify the addressing mode of the following instructions and explain them. (i) STA 6350H (ii) CMA (iii) MOV A,M (iv) MOV D,E (v) MVI A,A7H	*11*	*K3*	*CO2*
		OR			
	b)	Develop an ALP for 8085 microprocessor to add data stored in memory from 9200H.The first element in the location 9200H gives the number of elements in the array. Store the result of the addition in 9300H and 9301H.Assume the sum does not exceed 16 bits.	*11*	*K3*	*CO2*
25.	a)	Explain the architecture, functions and registers of the 8255 PPI.	*11*	*K2*	*CO3*
		OR			
	b)	Describe the internal architecture and programming of 8259 Programmable Interrupt Controller.	*11*	*K2*	*CO3*
26.	a)	Illustrate with a neat block diagram the architecture of 8051 microcontroller.	*11*	*K2*	*CO4*
		OR			
	b)	Explain the stepper motor control using 8051 and write an assembly language program for running the stepper motor in clockwise direction.	*11*	*K2*	*CO4*
27.	a)	Explain the concept of ARM cortex M0.	*11*	*K2*	*CO5*
		OR			
	b)	Recall the evolution of ARM processor from Acorn Ltd.	*11*	*K2*	*CO5*
28.	a) (i)	Explain the various program branching instructions available with 8051 microcontroller.	*6*	*K2*	*CO4*
	(ii)	Summarize the architectural block diagram of ARM cortex M0.	5	*K2*	*CO5*
		OR			
	b) (i)	Explain the following instructions of 8051 micro-controller. 1. DJNZ Ro, HERE 2. CJNZ @ Ri, #data, rel 3. SWAP A	*6*	*K2*	*CO4*
	(ii)	Explain about memory control block of ARM cortex M0.	5	*K2*	*CO5*