Reg. No.															

Question Paper Code	13401

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2025

Eight Semester

Electronics and Instrumentation Engineering

(Common to Instrumentation and Control Engineering)

20EIEL803 - VLSI DESIGN

Regulations - 2020

Duration: 3 Hours Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	*K – Level*	*CO*
1.	Parasitic capacitances are also called _____. (a) Depletion capacitance (b) Diffusion capacitance (c) Gate capacitance (d) Average Capacitance	*1*	*K1*	*CO1*
2.	Find the value of velocity if the voltage difference between drain and source is V_{ds}=4.3v, mobility for electrons in nMOS transistor is 510 cm^2/V and the channel length is 5cm. (a) 500units (b) 225 units (c) 438.6units (d) 200 units	*1*	*K2*	*CO1*
3.	CMOS domino logic occupies…….. (a) smaller area (b) larger area (c) Both smaller and larger area **(**d) None of the mentioned	*1*	*K1*	*CO2*
4.	Dynamic power depends on ____ (a) Sum of the effective capacitances of all the nodes (b) Sum of the gate capacitances of all the nodes (c) Sum of the diffusion capacitances of all the nodes (d) Sum of the wire capacitances of all the nodes	*1*	*K1*	*CO2*
5.	Race conditions can be avoided by keeping transparent period (a) long (b) zero (c) maximum (d) short	*1*	*K2*	*CO3*
6.	Sense amplifier generally employs …….. (a) negative feedback (b) positive feedback (c) neutral feedback (d) no feedback	*1*	*K1*	*CO3*
7.	The carry chain in adder is consist with… (a) cross-bar swith (b) transmission gate (c) bus interconncection (d) pass transistors	*1*	*K1*	*CO4*
8.	The delay of ripple carry adder is linearly proportional to…. (a) N (b) 2N (c) 2 (d) 8	*1*	*K2*	*CO4*
9.	Self-checking technique consists of …… (a) supplying coded input data (b) receiving coded output data (c) supplying all possible input sequence (d) all of the mentioned	*1*	*K1*	*CO5*
10.	The…… of FPGA consists of a 2-dimensional array of configurable logic blocks (CLBs) (a) Programmable logic structure (b) Programmable routing structure (c) Programmable Input/Output (I/O) (d) All of the mentioned	*1*	*K1*	*CO5*

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

11.	Outline the Lambda design rule.	*2*	*K2*	*CO1*
12.	Show the basic inverter circuit.	*2*	*K2*	*CO1*
13.	Compare constant field scaling and constant voltage scaling.	*2*	*K2*	*CO1*
14.	List the advantages of pass transistor.	*2*	*K1*	*CO2*
15.	Show a pseudo NMOS inverter.	*2*	*K2*	*CO2*
16.	Identify the applications of transmission gate.	*2*	*K3*	*CO2*
17.	Illustrate the circuit for generation two phase non overlapping clock.	*2*	*K2*	*CO3*
18.	Explain about pipelined operation.	*2*	*K2*	*CO3*

19.	Illustrate the equation for the propagation delay of N bit ripple carry adder.	*2*	*K2*	*CO4*
20.	Show why the partial sum adders are arranged in tree like fashion.	*2*	*K2*	*CO4*
21.	Compare the differences between standard IC and custom IC.	*2*	*K2*	*CO5*
22.	Interpret about antiques.	*2*	*K2*	*CO5*

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Explain the equation for source to drain current in the three regions of MOS transistor.	*11*	*K2*	*CO1*
		OR			
	b)	Summarize about the CV characteristics of MOS transistor along with neat sketches.	*11*	*K2*	*CO1*
24.	a)	Develop the Dual Rail Domino Logic families with necessary diagrams.	*11*	*K3*	*CO2*
		OR			
	b)	Apply the following power dissipation techniques and its impact in CMOS inverter circuits. (i) Static dissipation. (ii) Dynamic dissipation.	*11*	*K3*	*CO2*
25.	a)	Explain the various sources of clock skew and jitter with necessary diagrams.	*11*	*K2*	*CO3*
		OR			
	b)	Summarize about Multiplexer-Based Latches with neat diagram.	*11*	*K2*	*CO3*
26.	a)	Construct the Manchester carry chain adder with a neat diagram and supporting equations.	*11*	*K3*	*CO4*
		OR			
	b)	Build a booth multiplier with necessary diagrams and calculations.	*11*	*K3*	*CO4*
27.	a)	Explain the ASIC design flow with a neat diagram.	*11*	*K2*	*CO5*
		OR			
	b)	Summarize about the Boundary Scan in detail with supporting diagrams.	*11*	*K2*	*CO5*
28.	a) (i)	Build a Wallace tree multiplier and explain its working with neat diagrams.	*6*	*K3*	*CO4*
	(ii)	Illustrate Configurable Logic Blocks with neat diagrams.	*5*	*K2*	*CO5*
		OR			
	b) (i)	Construct a Carry Bypass adders and identify its delay equations.	*6*	*K3*	*CO4*
	(ii)	Illustrate Input output Block with neat diagrams.	*5*	*K2*	*CO5*