Reg. No.																

Question Paper Code	13605

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2025

Fourth semester

Electronics and Instrumentation Engineering

(Common to Instrumentation and Control Engineering)

20EIPW401 - DIGITAL ELECTRONICS WITH LABORATORY

Regulations - 2020

Duration: 3 Hours Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

No.	Question	Marks	K – Level	CO
1.	Convert the octal number $(4356)_8$ to Decimal number. (a) $(2276)_{10}$ (b) $(2286)_{10}$ (c) $(2176)_{10}$ (d) $(2186)_{10}$	1	K1	CO1
2.	In Boolean algebra, the bar sign (-) indicates ________________ (a) OR operation (b) AND operation (c) NOT operation (d) None of the above	1	K2	CO1
3.	Which gate is best used as a basic comparator? (a) NOR (b) OR (c) EX-OR (d) AND	1	K1	CO2
4.	The limiting factor on a speed of parallel adder is (a) Input delay (b) Carry propagation delay (c) Input propagation delay (d) Output delay	1	K2	CO2
5.	A ring counter is same as (a) Up-down counter (b) Parallel counter (c) Shift registers (d) None of above	1	K1	CO3
6.	A flip flop stores (a) 10 bit of information (b) 1 bit of information (c) 2 bit of information (d) 3-bit information	1	K2	CO3
7.	The number of flipflop required to build a Mod 15 counter is (a) 4 (b) 6 (c) 3 (d) 5	1	K1	CO4
8.	In DOWN-counter, each flip-flop is triggered by ___________ (a) Theoutput of the next flip-flop (b) The normal output of the preceding flip-flop (c) The clock pulse of the previous flip-flop (d) The inverted output of the preceding flip-flop	1	K2	CO4
9.	What does VHDL stand for? (a) Virtual Hardware Description Language (b) Very High-Speed Digital Logic (c) Very High-Speed Integrated Circuit Hardware Description Language (d) Variable High-Speed Device Language	1	K1	CO5
10.	In VHDL, an *entity* is used to: (a) Define the internal structure of a circuit (b) Specify inputs, outputs, and external ports of a circuit (c) Create simulation waveforms (d) Connect multiple processes	1	K2	CO5

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

No.	Question	Marks	K – Level	CO
11.	Name the universal gates. Why they are called so?	2	K1	CO1
12.	Write the truth table of Exclusive NOR gate and mention its applications.	2	K1	CO1
13.	Show how to connect NAND gates to get an AND gate and OR gate.	2	K2	CO1
14.	Write the truth table and expression for half adder.	2	K1	CO2
15.	Convert a 2 to 4 line decoder with enable input to 1x 4 demultiplexer.	2	K2	CO2

16.	Draw a 1:4 Demultiplexer using logic gates.	*2*	*K1*	*CO2*
17.	Draw the state table and excitation table of the T flip flop.	*2*	*K1*	*CO3*
18.	Differentiate between the edge triggering and level triggering.	*2*	*K2*	*CO3*
19.	Write the characteristic equation of a JK Flip flop.	*2*	*K1*	*CO4*
20.	Distinguish between Mealy and Moore machines.	*2*	*K2*	*CO4*
21.	List the operators present in VHDL.	*2*	*K1*	*CO5*
22.	Compare structural, behavioral, and data flow modelling in VHDL.	*2*	*K2*	*CO5*

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Construct and analyze the Karnaugh Map for the given function **F(A,B,C,D,E) = Σm(6,9,13,18,19,25,27,29,31) + Σd(2,3,11,15,17,24,28)** and illustrate the corresponding logic diagram.	*11*	*K2*	*CO1*
		OR			
	b)	Illustrate and explain the TTL logic circuit for a three-input NAND gate, highlighting its working principles.	*11*	*K2*	*CO1*
24.	a)	Design a Binary-to-Gray code converter and implement it using logic gates.	*11*	*K3*	*CO2*
		OR			
	b)	Explain 1:16 demultiplexer.	*11*	*K3*	*CO2*
25.	a) (i)	Explain the operation of JK flip flop with neat diagram.	*6*	*K3*	*CO3*
	(ii)	Convert to D flip-flop from a J-K flip-flop.	*5*	*K3*	*CO3*
		OR			
	b)	Explain the operation of master slave flip flop and show how the race around condition is eliminated.	*11*	*K3*	*CO3*
26.	a)	Apply the design of 4-bit BCD counter using T flip flops that counts in the following way: 0000,0001, 0010,0011,....,1001 and back to 0000 (i) Draw the state diagram. (ii) List the next state table. (iii) Draw the logic diagram of the circuit.	*11*	*K3*	*CO4*
		OR			
	b)	Construct a MOD-10 synchronous counter using JK flip flops. Write an execution table and state table.	*11*	*K3*	*CO4*
27.	a)	Illustrate the concept of structural modeling in VHDL by Designing a Full Adder as an example.	*11*	*K3*	*CO5*
		OR			
	b)	Create the behavioral and structural models of a 4-to-1 multiplexer in VHDL and test its working.	*11*	*K3*	*CO5*
28.	a) (i)	Explain in detail about critical races and non-critical races in asynchronous sequential circuits with examples.	*6*	*K3*	*CO4*
	(ii)	Discuss the role of a process statement in VHDL.	*5*	*K3*	*CO5*
		OR			
	b) (i)	Explain the concept, working, characteristics, implementation and application of PROM.	*6*	*K3*	*CO4*
	(ii)	Write the VHDL behavioral model for a T flip-flop.	*5*	*K3*	*CO5*