Reg. No.															

Question Paper Code	13735

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2025

Second Semester

Computer Science and Engineering

20ESIT203 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	A four variable Karnaugh map needs (a) 32 squares (b) 16 squares (c) 34 squares (d) 35 squares	1	K1	CO1
2.	Convert the octal number $(4356)_8$ to Decimal number. (a) $(2276)_{10}$ (b) $(2286)_{10}$ (c) $(2176)_{10}$ (d) $(2186)_{10}$	1	K1	CO1
3.	Carry generator in full adder has expression (a) G=AB (b) G=A+B (c) G=A-B (d) G=A/B	1	K1	CO2
4.	Which gate is best used as a basic comparator? (a) NOR (b) OR (c) EX-OR (d) AND	1	K1	CO2
5.	When an SR latch has S=1 and R=1, what will be the outcome? (a) 1 (b) 0 (c) Indeterminant (d) None of above	1	K1	CO3
6.	The basic storage element in a digital system is (a) Flip flop (b) Counter (c) Multiplexer (d) Decoder	1	K1	CO3
7.	Which of the following Verilog operators is used for logical AND? (a) && (b) & (c) | (d) ==	1	K1	CO4
8.	Which of the following HDLs is primarily used for designing digital circuits and systems? (a) Verilog (b) Python (c) C++ (d) Java	1	K1	CO4
9.	The race in which stable state depends on order is called (a) Critical race (b) Identical race (c) Non critical race (d) Defined race	1	K1	CO5
10.	PLDs with programmable AND and fixed OR arrays are called _____ (a) PAL (b) PLA (c) APL (d) PPL	1	K1	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

		Marks	K – Level	CO
11.	Convert binary 110111 into a decimal number system.	2	K2	CO1
12.	Define Absorption Theorem.	2	K1	CO1
13.	Define a Multiplexer.	2	K1	CO2
14.	State the function of the magnitude comparator.	2	K1	CO2
15.	Explain edge – triggered flip flop.	2	K2	CO3
16.	State the advantage of master slave flip flop.	2	K1	CO3
17.	Write a program for EX-OR gate using Verilog HDL.	2	K2	CO4
18.	State the uses of Hardware Description Language.	2	K1	CO4
19.	What is a non-criticalrace?	2	K1	CO5
20.	Define a merger graph.	2	K1	CO5
21.	Define programmable logic array. How does it differ from ROM?	2	K1	CO6
22.	Distinguish between EPROM and EEPROM.	2	K2	CO6

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	State and Explain various Boolean Algebraic laws.	*11*	*K2*	*CO1*
		OR			
	b)	Use Karnaugh Map method to reduce the following switching function and construct using LOGIC gates. F(A,B,C,D)=∑m(0,2,3,6,7). +∑d(8,10,11,15).	*11*	*K2*	*CO1*
24.	a)	Explain with neat diagram the function of 4-bit binary parallel adder and Subtractor.	*11*	*K2*	*CO2*
		OR			
	b)	Reduce the following Boolean function using 8:1 multiplexer. F (A, B, C, D) = ∑ (1, 3, 4, 11, 12, 13, 14, 15)	*11*	*K2*	*CO2*
25.	a)	Explain Universal Shift Register and the principle of Operation of 4-bit Universal Shift Register.	*11*	*K2*	*CO3*
		OR			
	b)	Explain the design and working of a synchronous mod – 3 counters.	*11*	*K2*	*CO3*
26.	a)	Discuss about 4-bit adder with gate level modelling and write a program using Verilog HDL.	*11*	*K2*	*CO4*
		OR			
	b)	Describe a full subtractor circuit and full adder circuit, write a code using Verilog HDL.	*11*	*K2*	*CO4*
27.	a)	Give the design Procedure for asynchronous sequential circuit.	*11*	*K3*	*CO5*
		OR			
	b)	Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input is transferred to Z. When Y is 0, the output does not change for any change in X.	*11*	*K3*	*CO5*
28.	a)	Design a functional circuit for F1=∑m(1,2) and F2=∑m(0,1,3) using ROM.	*11*	*K3*	*CO6*
		OR			
	b)	Use PLA to implement the following functions. A(x,y,z) = ∑m(1,2,4,6). B(x,y,z) = ∑m(0,1,6,7). C(x,y,z) = ∑m(2,6).	*11*	*K3*	*CO6*