				Reg	g. No.											
			Question Paper Co	ode 12335												
		ME/M	Fech - DEGREE EX		INATI	ONS	NC	V	/ DI	E <b>C 2</b>	202	3				
		141.12. / 141.	First	Seme	ester	0110,	110				02.	5				
			<b>M.E Big</b>	Data	Analy	tics										
		20P	BDPC103 – MULTI	ICOF	RE AR	СНІТ	<b>FEC</b>	TU	JRE	4						
			(Regula	ation	2020)											
Dur	ation	n: 3 Hours								Ma	x. N	Mark	cs: 1(	)0		
			PART - A (10	) × 2 =	= 20 M	(arks)	)									
			Answer A	LL Q	uestion	ıs							Ma	who		
1.	Wł	nat is response	e time?										<b>K-Lev</b> 2,K1	rks, el , CO ,CO1		
2.	Sta	te the need fo	r Instruction Level pa	aralle	lism.							2,K2,CO1				
3.	Cla	ussify two way	vs in which virtual ma	achin	e is har	ndled.							2,K2,CO2			
4.	Cla	ssify memory	hierarchy.										2,K2,CO2			
5.	Dif	fferentiate Bu	ses from crossbar net	work	s.							2,K2,CO3				
6.	Wł	nat is cache co	herence?									2,K1,CO3				
7.	Compare Homogeneous and heterogeneous multi-core architecture.									2,K2,CO4						
8.	De	fine cloud cor	nputing.									2,K1,CO4				
9.	Analyze the Vector functional units.								2,K2,CO5							
10.	Lis	t the Structura	al hazards in vectored	l arch	itectur	e.							2,K1,	,CO5		
			PART - B (5 >	× 13 =	= 65 M	arks)										
1 1	`		Answer A		Juestion	ıs		1 4	•1				12 V:	2 CO1		
11.	a)	Draw and E	xplain the SMT and C	CMP	Archite	ecture	: 1n (	deta	a11.				15,65	,001		
			0	DR												
	b)	Summarize and the limi	in details about the va tations of ILP.	ariou	s depen	dence	es ca	aus	es iı	ı ILI	)		13,K3	,CO1		
12.	a)	Express in d	etail about the optim	izatic	ons of c	ache	perf	orn	nano	e.			13, K4	,CO2		
			0	R												
	b)	(i) Explain	in detail about Virtua	l Me	mory.			1	•,				06,K2	,CO2		
		(11) List the	memory technologies	s usec	1 in Coi	mpute	r A	rch	1tec	ure.			07,K2	,CO2		
13.	a)	Analyze the	role of cache coheren	nce ir	n multij	proces	ssor	•					13,K4	,CO3		
														-		

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create 12335

	b)	<ul><li>(i) Describe Multistage Interconnection Networks.</li><li>(ii) Explain the Bus Network.</li></ul>						
14.	a)	Describe the following topics: (i) Homogenous Multi-core architecture. (ii) Heterogeneous Multi-core architecture.						
OR								
	b)	Explain in detail the Computer Architectural details of Warehouse Scale Computers.	13,K3,CO4					

OR

15. a) (i) Analyze the basic Graphics processing Units.07,K3,C05(ii) Explain the details of GPGPU computing.06,K3,C05

## OR

b) Identify the need for SIMD Extension for multimedia and explain with <sup>13,K3,CO5</sup> an example.

## PART C $(1 \times 15 = 15 \text{ Marks})$

16. a) Explain the primary components of instruction set architecture of <sup>15,K2,CO6</sup> AMIPS and explain vector architecture.

## OR

b) Explain the issues in finding dependencies and eliminating dependent <sup>15,K2,CO6</sup> computation.