Reg. No.												

Question Paper Code	12315

M.E. / M.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2023

First Semester

M.E. - Computer Science and Engineering

(Common to M.E. - Computer Science and Engineering (with Specialization in Networks))

20PCNPC101 - ADVANCED COMPUTER ARCHITECTURE

(Regulations 2020)

Duration: 3 Hours Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	List out the Limitations of ILP.	*2,K1,CO1*
2.	Differentiate coarse grained and fine grained multithreading.	*2,K2,CO1*
3.	Compare Scalar and Vector processors.	*2,K2,CO2*
4.	Define dependency and list its types.	*2,K1,CO2*
5.	Illustrate spin locks.	*2,K2,CO3*
6.	What is the need of multiprocessor?	*2,K1,CO3*
7.	What do you mean by airside economization?	*2,K1,CO4*
8.	Summarize the Power Utilization effectiveness.	*2,K2,CO4*
9.	Extend the term - Thread block.	*2,K2,CO5*
10.	Contrast scalar registers and Vector registers.	*2,K2,CO5*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Discuss how hardware based speculation is used to overcome control dependence.	*13,K2,CO1*
		OR	
	b)	What is ILP? Discuss about the types of dependencies with example.	*13,K2,CO1*
12.	a)	Explain the virtual memory translation and TLB with necessary diagram.	*13,K2,CO2*
		OR	
	b)	What is memory hierarchy? Elaborate the level in memory hierarchy with a diagram.	*13,K2,CO2*
13.	a)	Explain Synchronization and Classify Multicomputer from Multiprocessors.	*13,K2,CO3*

OR

b) Examine Implementing Locks Using Coherence. *13,K2,CO3*

14. a) (i) Summarize the Efficiency of a WSC. *7,K2,CO4*
(ii) Describe the Capital expenditures (CAPEX). *6,K2,CO4*

OR

b) What do you mean by Warehouse-scale computers and Describe about a Batch processing framework. *13,K3,CO4*

15. a) (i) Demonstrate the factors in Eliminating dependent computations *7,K2,CO5*
(ii) Explain the basic structure of a vector architecture VMIPS. *6,K2,CO6*

OR

b) (i) Summarize the elements of Graphics processing Units. *7,K2,CO5*
(ii) Discuss the concept of Multiple Lanes: Beyond One Element per Clock Cycle. *6,K2,CO6*

PART - C (1 × 15 = 15 Marks)

16. a) Develop any four multicore architectures which you have studied, analyze the advantages and disadvantages and present a summary of it. *15,K3,CO6*

OR

b) (i) Explain the details of handling Multidimensional Arrays in Vector Architectures. *8,K3,CO6*
(ii) Identify how to Handle Sparse Matrices in Vector Architectures. *7,K3,CO6*

.