Reg. No.												

Question Paper Code	12317

M.E. / M.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2023

First Semester

M.E. - Embedded Systems Technologies

20PESPC101 - ADVANCED DIGITAL PRINCIPLES AND DESIGN

(Regulations 2020)

Duration: 3 Hours Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	Recollect the Characteristic equation and table of JK flip flop.	*2,K1,CO1*
2.	Recall the excitation table for JK flipflop.	*2,K1,CO1*
3.	Bring out the importance of state reduction.	*2,K2,CO2*
4.	Give the reduced state table in the design of sequential circuits for minimizing the hardware.	*2,K2,CO2*

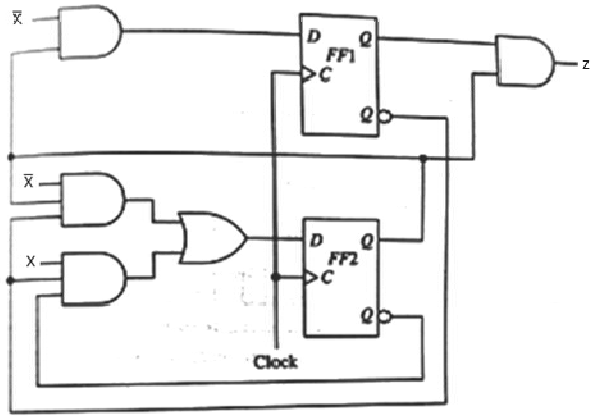
Present state	Next state	Next state	Output Z1	Outputz2
a	d	b	0	0
b	e	a	0	0
c	g	f	0	1
d	a	d	1	0
e	a	b	1	0
f	d	b	0	0
g	a	e	1	0

5.	Bring out the difference between the stuck at 0 and stuck at 1 fault.	*2,K2,CO3*
6.	State the importance of Built in Self Test.	*2,K1,CO3*
7.	Differentiate between PAL and PLA.	*2,K2,CO4*
8.	List the important features of Xilinx FPGA family.	*2,K1,CO4*
9.	Outline the advantage of reconfigurable logic designs.	*2,K2,CO5*
10.	State the advantages of CLBs.	*2,K1,CO5*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Illustrate the Transition table, Excitation table, state table and state diagram for the following synchronous sequential circuit and	*13,K2,CO1*



OR

b) An Asynchronous sequential circuit is given by the following excitation and output function

$Y1 = x_1x_2 + x_1y_2+x_2y_1$

$Y_2 = x_2+x_1y_1y_2 +x_1y_1$

$Z = x_2+y_1$

(i) Draw the logic diagram of the circuit. *8,K2,CO1*

(ii) Derive the transition table and output map. *5,K2,CO1*

12. a) In the design a network produces a 1 if and only if the current input and the previous 3 inputs correspond to either of the sequence 1001 or 0110. The one output occurs at the time of fourth input of the recognized sequence. Output of 0 is to be produced at all other times and the sequences are allowed to overlap. Give the state diagram and the reduced state table. *13,K3,CO2*

OR

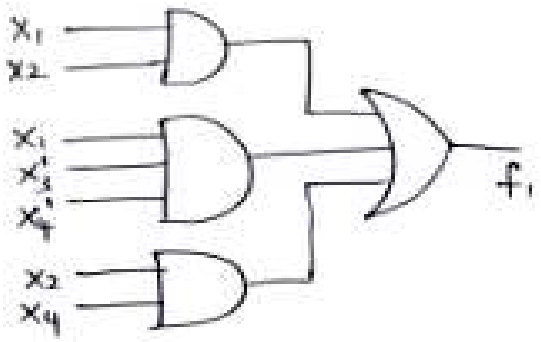
b) Design a 0110/1001 sequence detector. Give the state diagram and the reduced state table. *13,K3,CO2*

13. a) Derive the primitive flow table and state Diagram for the system with inputs X and Y and output Z. *13,K2,CO3*

Initially both inputs and outputs are 0. If X = 1 and Y = 0 output Z=1. When X = 0 and Y = 1 output Z=0.If X = Y = 0 or X = Y = 1 then output Z has no change. The logic system has edge triggered input and any static inputs will not have any effect on the system output Z.

OR

b) For a given diagram, find a-test using kohavi algorithm to find faults in x1. *13,K2,CO3*



14. a) Discuss in detail the interconnects and memory architecture of Xilinx 2000 with necessary diagram. *13,K2,CO4*

OR

b) Explain in detail the Programmable Electrically Erasable Logic and the different Programming Techniques. *13,K2,CO4*

15. a) A combinational logic circuit is defined by the function given below. Implement the circuit using Programmable Array Logic. *13,K2,CO5*

F(R,S,T,U) = $\sum(3,5,7,14,15)$

$G(\mathrm{R,S,T,U}) = \sum(3,4,5,7,10)$

OR

b) Implement the following Boolean function using Programmable Logic Array. *13,K2,CO5*

W(A, B, C, D) = $\sum(0,2,6,7,8,9,12,13)$

$X(\mathrm{A,B,C,D}) = \sum(0,2,6,7,8,9,12,13,14)$

Y(A, B, C, D) = $\sum(2,3,8,9,10,12,13)$

$Z(\mathrm{A,B,C,D}) = \sum(1,3,4,6,9,12,14)$

PART - C (1 × 15 = 15 Marks)

16. a) Analyze the operation of 4:1 Multiplexer and compare the VHDL programming model of the same. *15,K4,CO6*

OR

b) Compare and contrast the structural and behavioral modeling of VHDL with suitable examples. *15,K4,CO6*