Reg. No.												

Question Paper Code	12220

B.E. / B.Tech - DEGREE EXAMINATIONS, NOV / DEC 2023

Sixth Semester

Electronics and Communication Engineering

EC8095 - VLSI DESIGN

(Regulations 2017)

Duration: 3 Hours Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	Define Body bias effect.	*2,K1,CO1*
2.	What are the objectives of Layout rules and write its types.	*2,K1,CO1*
3.	Implement a 2:1 multiplexer using pass transistor.	*2,K2,CO2*
4.	Sketch the sense amplifier based CMOS circuit.	*2,K2,CO2*
5.	Compare and contrast synchronous design and asynchronous design.	*2,K1,CO3*
6.	Define Clock Skew.	*2,K1,CO3*
7.	Why is barrel shifter very useful in the designing of arithmetic circuits?	*2,K1,CO4*
8.	Determine the propagation delay of n-bit Ripple Carry Adder.	*2,K2,CO4*
9.	Name any two types of routing in FPGA.	*2,K2,CO5*
10.	What are feed through cells? State their uses.	*2,K2,CO5*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Draw the CMOS inverter and discuss its DC characteristics. Write the conditions for the different regions of operations.	*13,K2,CO1*
		OR	
	b)	Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistors.	*13,K2,CO1*
12.	a)	Explain the properties and operation of dynamic CMOS logic with neat diagram.	*13,K2,CO2*
		OR	
	b)	Illustrate the Schmitt trigger and explain its CMOS implementation with neat diagram.	*13,K2,CO2*

13. a) Analyze clock skew, clock jitter and explain its combined impact in detail. *13,K3,CO3*

OR

b) Examine the timing basics and explain the clock distribution techniques in synchronous design in detail. *13,K3,CO3*

14. a) Design a 4X4 array multiplier and write down the equation for delay with appropriate diagram. *13,K3,CO4*

OR

b) Design a 4 bit barrel shifter and Logarithmic shifter and explain its operation in detail. *13,K3,CO4*

15. a) Explain in detail about the FPGA building block architectures with neat diagram. *13,K2,CO5*

OR

b) With neat Sketch explain the CLB, IOB and programmable interconnects of an FPGA device. *13,K2,CO5*

PART - C (1 × 15 = 15 Marks)

16. a) Compare the architecture of different scan based testing method of CMOS circuits. *15,K3,CO6*

OR

b) Draw the block diagram of BILBO\BIST and explain each unit operation. *15,K3,CO6*