Reg. No.												

Question Paper Code	12590

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2024

Sixth Semester

Electronics and Communication Engineering

EC8095 - VLSI DESIGN

Regulation - 2017

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	Define threshold voltage.	2	K1	CO1
2.	Describe the channel length modulation.	2	K1	CO1
3.	Write short notes on CVSL.	2	K2	CO2
4.	List the factors that cause static power dissipation in CMOS circuits	2	K1	CO2
5.	Differentiate arithmetic and barrel shifter.	2	K2	CO3
6.	Construct the block diagram of carry chain adder.	2	K2	CO3
7.	Write the charge - share equation of DRAM.	2	K1	CO4
8.	Define Fuse based FGPA.	2	K1	CO4
9.	Outline the limitations of IDDQ testing.	2	K2	CO5
10.	List the common techniques for ad hoc testing.	2	K1	CO5

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

			Marks	K – Level	CO
11.	a)	Explain the operation of NMOS enhancement transistor with neat diagram and write current equations in all three regions.	13	K2	CO1
		OR			
	b)	Explain & derive the expressions for effective resistance and capacitance estimation using Elmore's RC delay model.	13	K2	CO1
12.	a)	Illustrate the operation of pass transistor logic and transmission gates.	13	K3	CO2
		OR			
	b)	Illustrate the operation of dynamic CMOS domino and NP domino logic with necessary diagrams.	13	K3	CO2
13.	a)	Explain about the DRAM sub array and open bit lines architecture.	13	K3	CO3
		OR			
	b)	Analyze the FPGA interconnect routing procedures.	13	K3	CO3

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create

14.	a)	Construct a array multiplier for 4 bit by 4 bit. Explain its operation and summarize the number of adders.	*13*	*K3*	*CO4*
		OR			
	b)	Sketch & explain various types of shifters and write its applications.	*13*	*K3*	*CO4*
15.	a)	Explain the factors to ne considered to optimize circuits for manufacturability.	*13*	*K4*	*CO5*
		OR			
	b)	Analyze Built in self test (BIST) with an example.	*13*	*K2*	*CO5*

PART - C (1 × 15 = 15 Marks)

16.	a)	Analyze the pipelining concepts in latches and registers.	*15*	*K3*	*CO6*
		OR			
	b)	Examine monostable sequential circuits & astable circuits with an example.	*15*	*K2*	*CO6*