| Reg. No. | | | | | | | | | | | | | | | | |
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| Question Paper Code | 14062 |
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**B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025**

Fifth Semester

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**20ECPC502 - VLSI DESIGN**

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

**PART - A (MCQ) (10 × 1 = 10 Marks)**

Answer ALL Questions

| | | Marks | K – Level | CO |
|---|---|---|---|---|
| 1. | Which of the following transistor is conducting in non-saturation region of CMOS inverter?<br>(a) nMOS (b) pMOS<br>(c) both nMOS and pMOS (d) None of the mentioned | 1 | K2 | CO1 |
| 2. | The RC delay model is used to estimate:<br>(a) Power consumption of a circuit (b) Clock frequency of a circuit<br>(c) Propagation delay of signals (d) Static power dissipation of a circuit | 1 | K1 | CO1 |
| 3. | Double pass transistor logic like…….. is a dual-rail logic family which produces true and complement logic outputs from each stage.<br>(a) Complementary Pass transistor logic<br>(b) Differential cascode voltage switch with pass-gate logic<br>(c) Both complementary pass transistor logic and differential cascode voltage switch with pass-gate<br>(d) None of the mentioned | 1 | K2 | CO2 |
| 4. | P/N ratio is not dependent on which of the following factors.<br>(a) area (b) power<br>(c) reliability (d) average delay | 1 | K1 | CO2 |
| 5. | The difference between the positions of the rising edges of the clock with respect to a reference is called _____.<br>(a) clock skew (b) clock jitter (c) delay (d) none of the mentioned | 1 | K2 | CO3 |
| 6. | Which of the following clocking increases overall performance?<br>(a) latch based clocking (b) register based clocking<br>(c) transistor based clocking (d) none of the mentioned | 1 | K2 | CO3 |
| 7. | The stimulus block in Verilog is used for:<br>(a) Applying test inputs to the design (b) Describing the design module<br>(c) Performing synthesis (d) Setting gate delays | 1 | K1 | CO4 |
| 8. | The keyword wire is used to:<br>(a) Store a value (b) Connect components together<br>(c) Represent sequential logic (d) Define a register variable | 1 | K1 | CO4 |
| 9. | The carry look ahead adder solves the……. problem.<br>(a) carry delay (b) Ripple carry<br>(c) n-bit parallel (d) Carry skip | 1 | K2 | CO5 |
| 10. | Circuits that can hold their state as long as power is applied is _____<br>(a) Dynamic memory (b) Static Memory (c) Register (d) Cache | 1 | K1 | CO6 |

**PART - B (12 × 2 = 24 Marks)**

Answer ALL Questions

| | | Marks | K – Level | CO |
|---|---|---|---|---|
| 11. | How PMOS and NMOS act as a switch? | 2 | K1 | CO1 |
| 12. | Mention the effects of channel length modulation on I-V behavior. | 2 | K1 | CO1 |
| 13. | Realize the two-input NAND gate using pass transistor logic. | 2 | K2 | CO2 |
| 14. | Compare the static CMOS and Pseudo-nMOS inverters. | 2 | K2 | CO2 |

| | | | | | |
|---|---|---|---|---|---|
| 15. | Define Bistability principle. | *2* | *K1* | *CO3* |
| 16. | What are the timing Classification of Digital systems? | *2* | *K1* | *CO3* |
| 17. | How do you specify delay in continuous assignments? | *2* | *K1* | *CO4* |
| 18. | Distinguish between structural and switch level modeling. | *2* | *K2* | *CO4* |
| 19. | What is the data path of the processor? State its functions. | *2* | *K1* | *CO5* |
| 20. | Describe booth's recoding. | *2* | *K2* | *CO5* |
| 21. | Draw a one Transistor Dynamic RAM cell. | *2* | *K2* | *CO6* |
| 22. | What are the main advantages of using a hierarchical memory organization? | *2* | *K1* | *CO6* |

**PART - C (6 × 11 = 66 Marks)**

Answer ALL Questions

| | | | | | | |
|---|---|---|---|---|---|---|
| 23. | a) | Elaborate about the CV characteristics of MOS transistor along with neat sketches. | *11* | *K2* | *CO1* |
| | | **OR** | | | |
| | b) | Explain the DC Transfer characteristics of a CMOS inverter and describe the different regions of operation. | *11* | *K2* | *CO1* |
| 24. | a) | Apply the concept of CMOS logic to describe the operation of a Cascode Voltage Switch Logic (CVSL) circuit. | *11* | *K3* | *CO2* |
| | | **OR** | | | |
| | b) (i) | Draw the CMOS logic circuit for the Boolean expression $Z = [(A + B)(A + C)(B + D)]'$ . | *6* | *K3* | *CO2* |
| | (ii) | Analyze the limitations of dynamic logic and apply suitable design techniques to overcome these issues. | *5* | *K3* | *CO2* |
| 25. | a) | Describe the different components of power dissipation in CMOS circuits. | *11* | *K2* | *CO3* |
| | | **OR** | | | |
| | b) | Draw and explain about Master-Slave Edge-Triggered register with its timing properties and non-ideal clock signals. | *11* | *K2* | *CO3* |
| 26. | a) | Construct a Verilog program for 3:8 decoder using any one modeling technique. | *11* | *K3* | *CO4* |
| | | **OR** | | | |
| | b) | Write a Verilog program using continuous assignment to implement a full adder with propagation delay and explain the code. | *11* | *K3* | *CO4* |
| 27. | a) | Illustrate the working of carry bypass adder and linear carry-select adder with neat diagrams. | *11* | *K3* | *CO5* |
| | | **OR** | | | |
| | b) | Analyze the principle behind Logarithmic and Barrel shifter with neat sketches. | *11* | *K3* | *CO5* |
| 28. | a) | Explain the memory architecture and its control circuits in detail. | *11* | *K2* | *CO6* |
| | | **OR** | | | |
| | b) | Explain the sub-circuits involved in Memory peripheral circuitry in detail with neat sketches of all the sub-circuits. | *11* | *K2* | *CO6* |